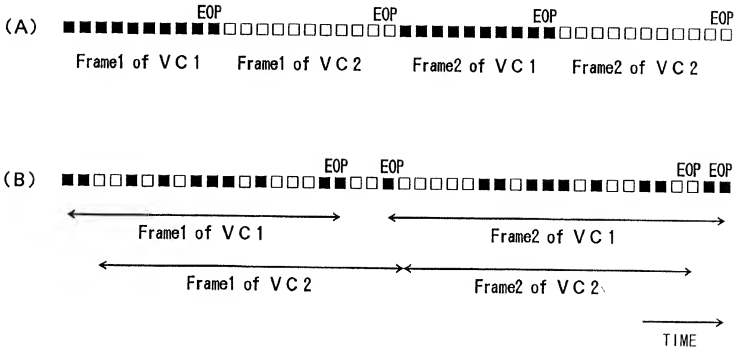
# FIG. 1


(A)
EOP
EOP
EOP
EOP
Frame1 of VC1
Frame1 of VC2
Frame2 of VC1
Frame2 of VC2
(B)
EOP
EOP
EOP EOP
Frame1 of VC1
Frame2 of VC1
Frame1 of VC2
Frame2 of VC2
TIME

# FIG.2

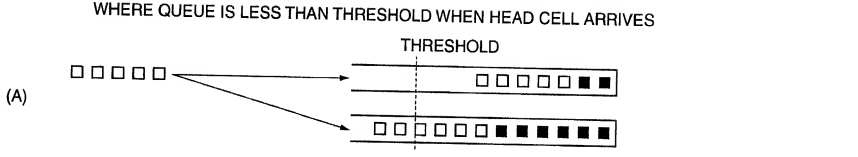

WHERE QUEUE IS LESS THAN THRESHOLD WHEN HEAD CELL ARRIVES
THRESHOLD
(A)
ALL CELLS IN FRAME INPUTTED WHETHER OR NOT THRESHOLD IS EXCEEDED DURING INPUT
WHERE QUEUE EXCEEDS THRESHOLD WHEN HEAD CELL ARRIVES
(B)
DISCARD ALL CELLS IN FRAMES, FROM HEAD CELL TO END CELL

FIG.3

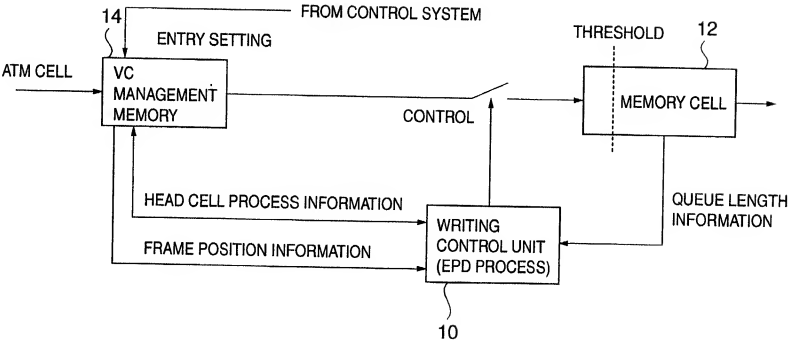

14
FROM CONTROL SYSTEM
ENTRY SETTING
ATM CELL
VC
MANAGEMENT
MEMORY
CONTROL
THRESHOLD
12
MEMORY CELL
HEAD CELL PROCESS INFORMATION
FRAME POSITION INFORMATION
WRITING
CONTROL UNIT
(EPD PROCESS)
QUEUE LENGTH
INFORMATION
10

FIG.4

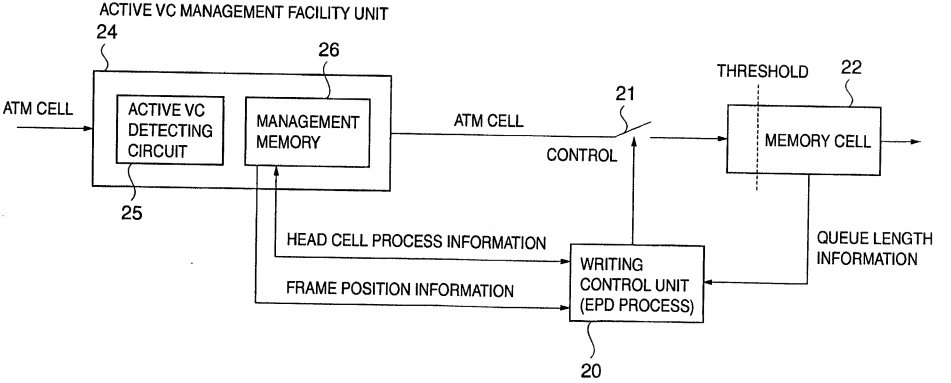

ACTIVE VC MANAGEMENT FACILITY UNIT
24
26
ATM CELL
ACTIVE VC DETECTING CIRCUIT
MANAGEMENT MEMORY
25
ATM CELL
21
CONTROL
THRESHOLD
22
MEMORY CELL
HEAD CELL PROCESS INFORMATION
FRAME POSITION INFORMATION
WRITING CONTROL UNIT (EPD PROCESS)
20
QUEUE LENGTH INFORMATION

FIG.5

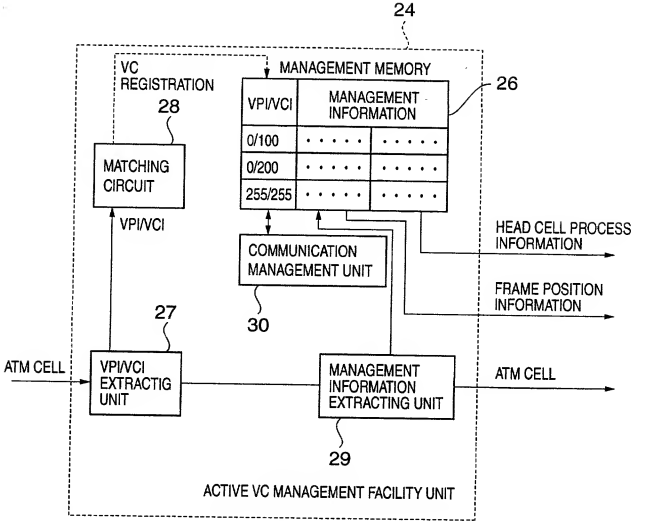

24
VC REGISTRATION
MANAGEMENT MEMORY
28
26
VPI/VCI
MANAGEMENT INFORMATION
0/100
0/200
255/255
MATCHING CIRCUIT
VPI/VCI
HEAD CELL PROCESS INFORMATION
COMMUNICATION MANAGEMENT UNIT
FRAME POSITION INFORMATION
27
30
ATM CELL
VPI/VCI EXTRACTIG UNIT
MANAGEMENT INFORMATION EXTRACTING UNIT
ATM CELL
29
ACTIVE VC MANAGEMENT FACILITY UNIT

FIG.6

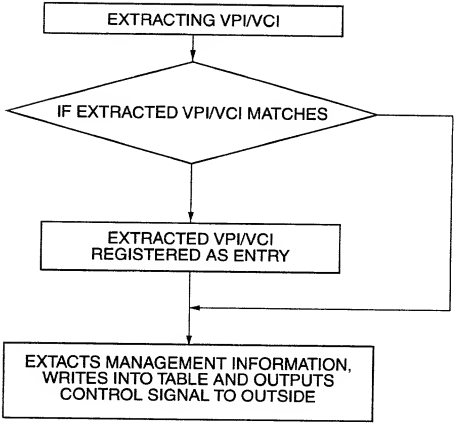

EXTRACTING VPI/VCI
IF EXTRACTED VPI/VCI MATCHES
EXTRACTED VPI/VCI REGISTERED AS ENTRY
EXTACTS MANAGEMENT INFORMATION, WRITES INTO TABLE AND OUTPUTS CONTROL SIGNAL TO OUTSIDE

FIG.7

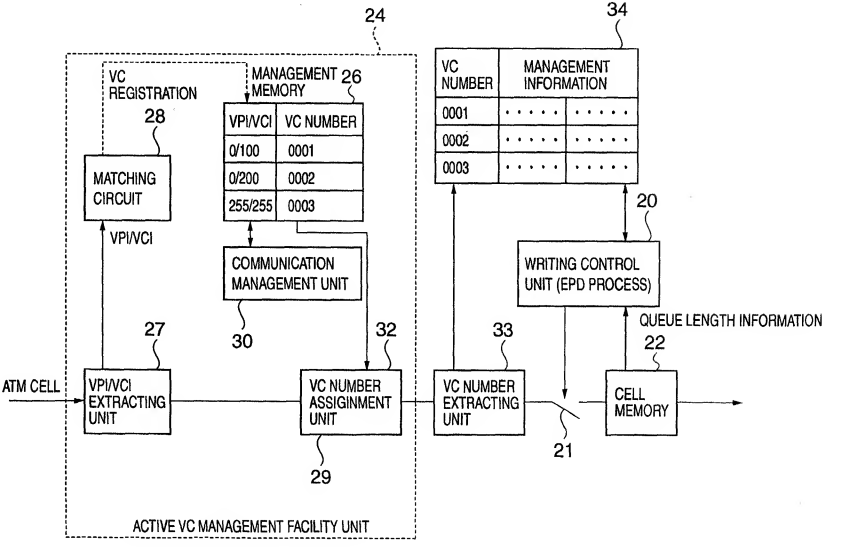

24
34
VC REGISTRATION
MANAGEMENT MEMORY
26
28
VPI/VCI
VC NUMBER
0/100
0001
0/200
0002
255/255
0003
MATCHING CIRCUIT
VPI/VCI
COMMUNICATION MANAGEMENT UNIT
30
VC NUMBER
MANAGEMENT INFORMATION
0001
0002
0003
20
WRITING CONTROL UNIT (EPD PROCESS)
QUEUE LENGTH INFORMATION
22
27
32
33
ATM CELL
VPI/VCI EXTRACTING UNIT
VC NUMBER ASSIGINMENT UNIT
VC NUMBER EXTRACTING UNIT
CELL MEMORY
21
29
ACTIVE VC MANAGEMENT FACILITY UNIT

FIG.8

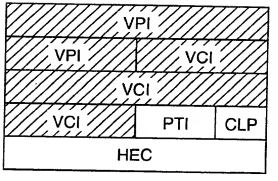


FIG.9

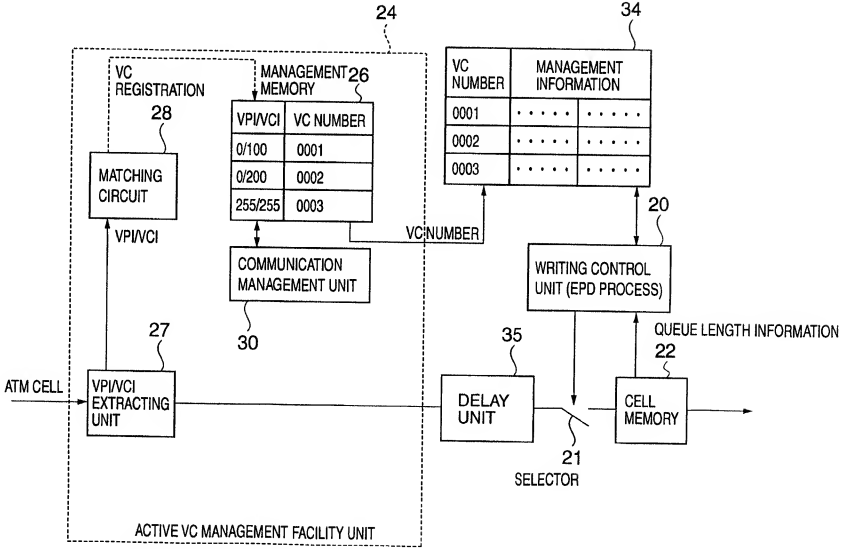

24
34
VC REGISTRATION
MANAGEMENT MEMORY
26
VC NUMBER
MANAGEMENT INFORMATION
0001
0002
0003
28
VPI/VCI
VC NUMBER
0/100
0001
0/200
0002
255/255
0003
MATCHING CIRCUIT
VPI/VCI
VC NUMBER
20
COMMUNICATION MANAGEMENT UNIT
WRITING CONTROL UNIT (EPD PROCESS)
30
27
35
QUEUE LENGTH INFORMATION
22
ATM CELL
VPI/VCI EXTRACTING UNIT
DELAY UNIT
CELL MEMORY
21
SELECTOR
ACTIVE VC MANAGEMENT FACILITY UNIT

FIG.10

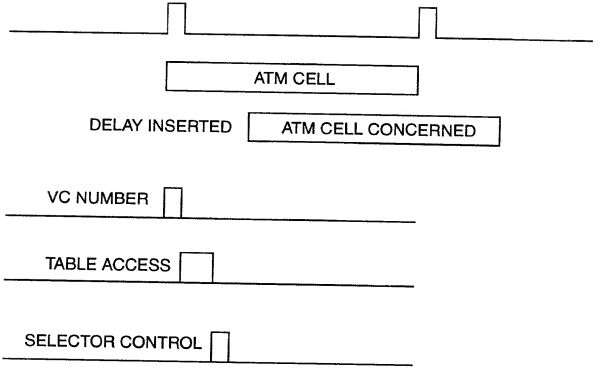



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FIG.11

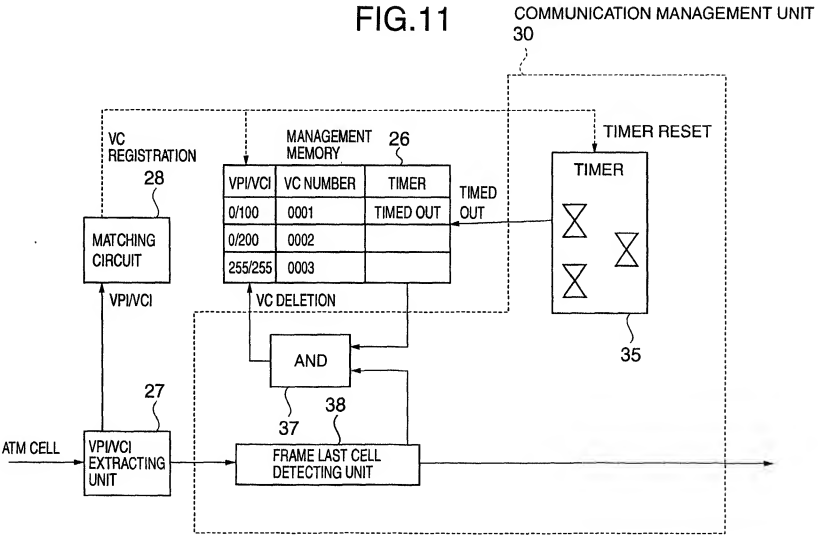
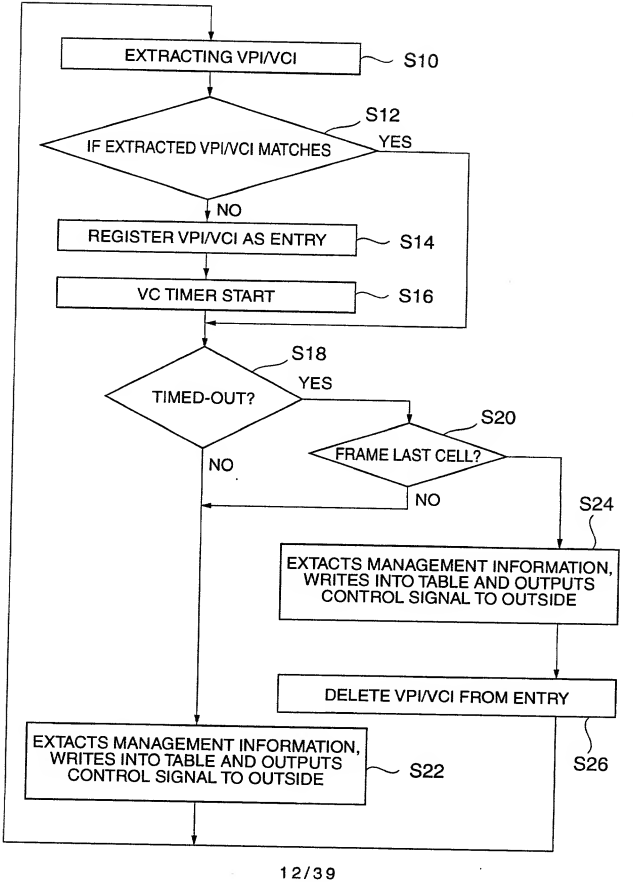

COMMUNICATION MANAGEMENT UNIT
30
VC
REGISTRATION
28
MANAGEMENT
MEMORY
26
TIMER RESET
TIMER
VPI/VCI
VC NUMBER
TIMER
0/100
0001
TIMED OUT
0/200
0002
255/255
0003
TIMED
OUT
MATCHING
CIRCUIT
VPI/VCI
VC DELETION
AND
35
27
37
38
ATM CELL
VPI/VCI
EXTRACTING
UNIT
FRAME LAST CELL
DETECTING UNIT

FIG.12


EXTRACTING VPI/VCI
S10
S12
IF EXTRACTED VPI/VCI MATCHES
YES
NO
REGISTER VPI/VCI AS ENTRY
S14
VC TIMER START
S16
S18
TIMED-OUT?
YES
S20
FRAME LAST CELL?
NO
NO
S24
EXTACTS MANAGEMENT INFORMATION, WRITES INTO TABLE AND OUTPUTS CONTROL SIGNAL TO OUTSIDE
DELETE VPI/VCI FROM ENTRY
S26
EXTACTS MANAGEMENT INFORMATION, WRITES INTO TABLE AND OUTPUTS CONTROL SIGNAL TO OUTSIDE
S22

JP2001274801A

FIG.13

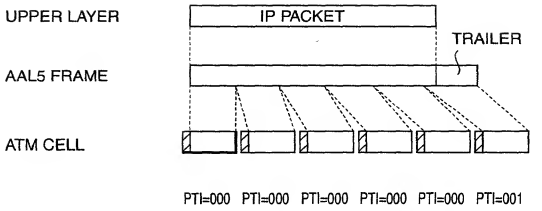


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FIG.14

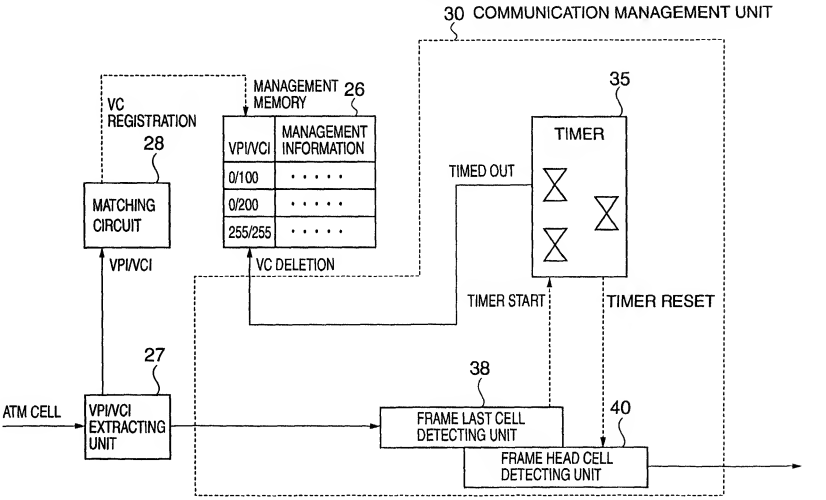
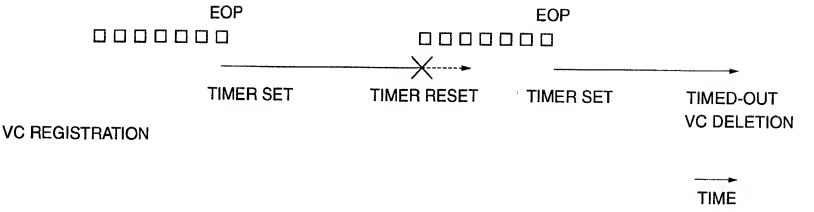


FIG.15


EOP
EOP
TIMER SET
TIMER RESET
TIMER SET
TIMED-OUT
VC DELETION
VC REGISTRATION
TIME

TOKYO 6E062001

FIG.16

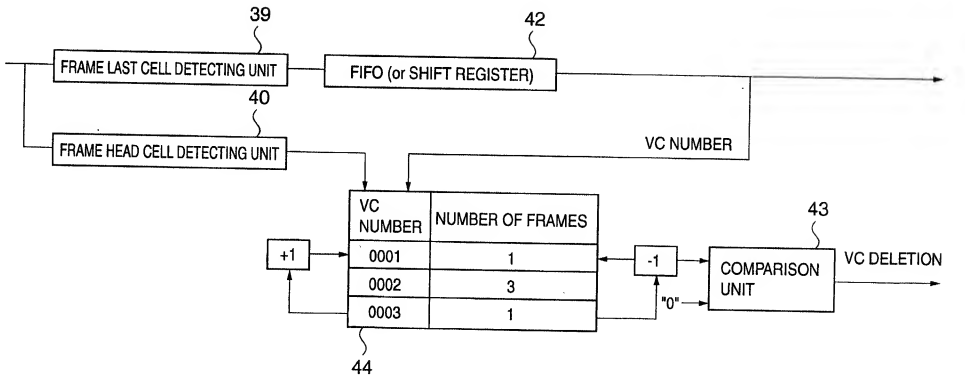
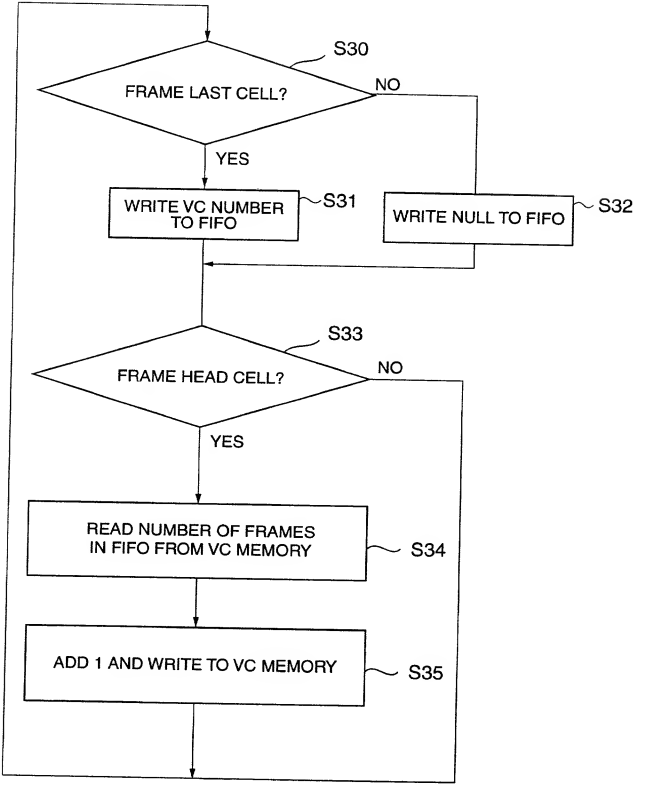
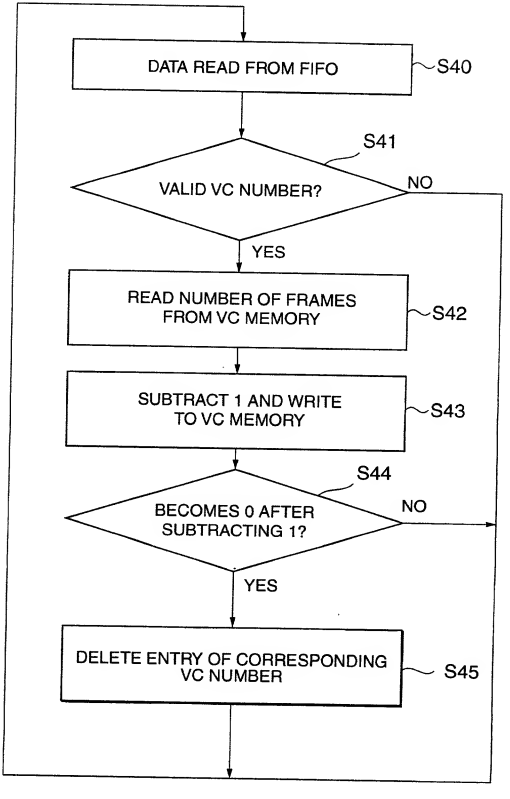


FIG.17




Patent Application

FIG.18


DATA READ FROM FIFO
S40
S41
VALID VC NUMBER?
NO
YES
READ NUMBER OF FRAMES FROM VC MEMORY
S42
SUBTRACT 1 AND WRITE TO VC MEMORY
S43
S44
BECOMES 0 AFTER SUBTRACTING 1?
NO
YES
DELETE ENTRY OF CORRESPONDING VC NUMBER
S45

TOHIZI' 6EH62001

FIG.19

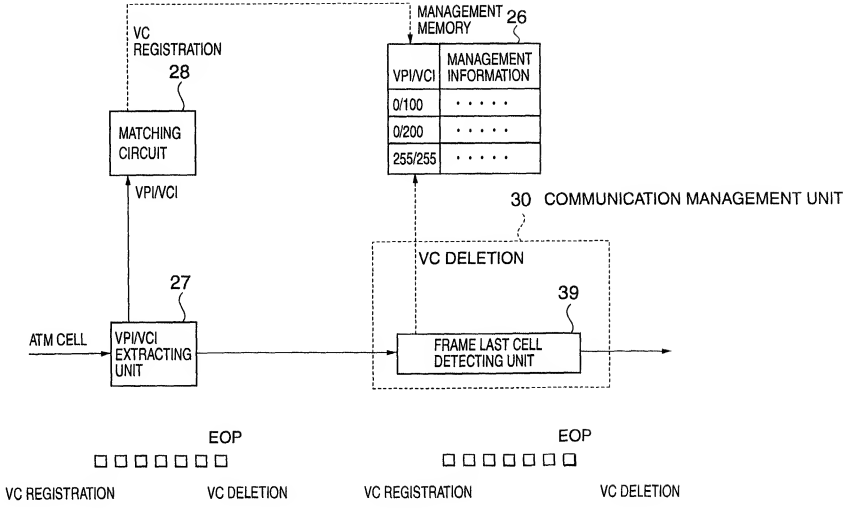


FIG.20

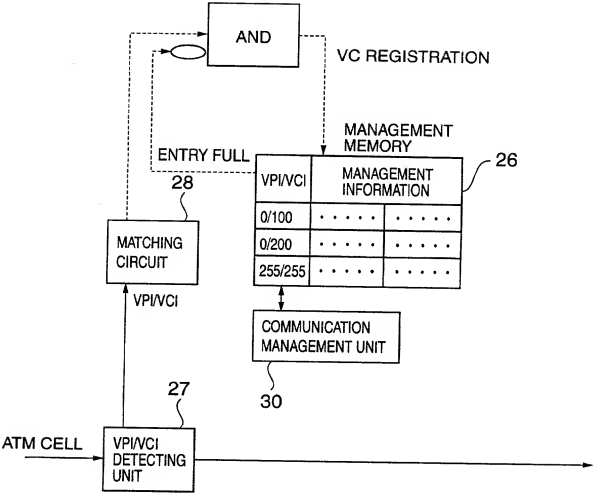

AND
VC REGISTRATION
MANAGEMENT MEMORY
ENTRY FULL
28
VPI/VCI
MANAGEMENT INFORMATION
26
0/100
0/200
255/255
MATCHING CIRCUIT
VPI/VCI
COMMUNICATION MANAGEMENT UNIT
30
27
ATM CELL
VPI/VCI DETECTING UNIT

FIG.21

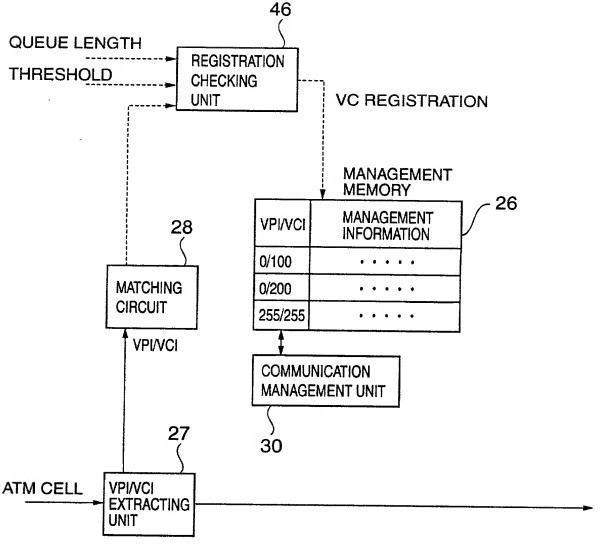

46
QUEUE LENGTH
THRESHOLD
REGISTRATION CHECKING UNIT
VC REGISTRATION
MANAGEMENT MEMORY
26
VPI/VCI
MANAGEMENT INFORMATION
0/100
0/200
255/255
28
MATCHING CIRCUIT
VPI/VCI
COMMUNICATION MANAGEMENT UNIT
30
27
ATM CELL
VPI/VCI EXTRACTING UNIT

FIG.22

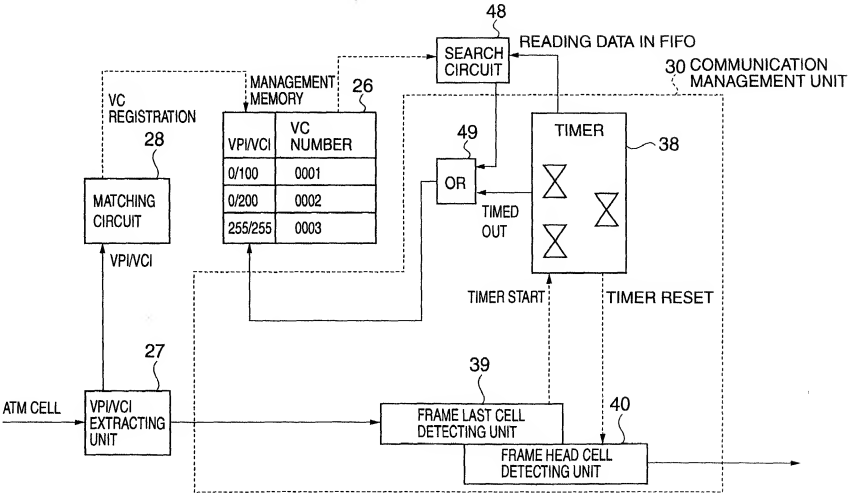

48
SEARCH CIRCUIT
READING DATA IN FIFO
30 COMMUNICATION MANAGEMENT UNIT
MANAGEMENT MEMORY
26
VC REGISTRATION
28
VPI/VCI
VC NUMBER
0/100
0001
0/200
0002
255/255
0003
49
OR
TIMER
38
TIMED OUT
MATCHING CIRCUIT
VPI/VCI
TIMER START
TIMER RESET
27
39
40
ATM CELL
VPI/VCI EXTRACTING UNIT
FRAME LAST CELL DETECTING UNIT
FRAME HEAD CELL DETECTING UNIT

FIG.23

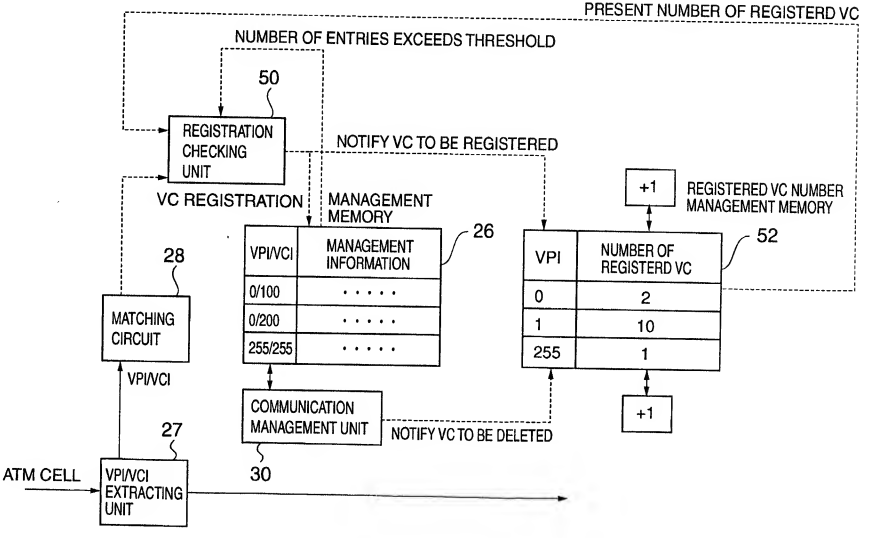
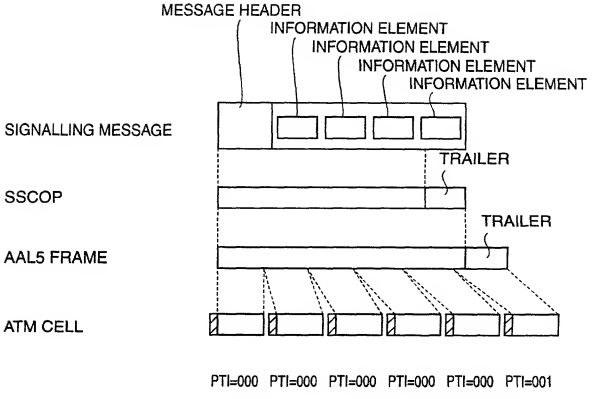

PRESENT NUMBER OF REGISTERD VC
NUMBER OF ENTRIES EXCEEDS THRESHOLD
50
REGISTRATION CHECKING UNIT
NOTIFY VC TO BE REGISTERED
+1
REGISTERED VC NUMBER MANAGEMENT MEMORY
VC REGISTRATION
MANAGEMENT MEMORY
26
52
28
VPI/VCI
MANAGEMENT INFORMATION
VPI
NUMBER OF REGISTERD VC
0/100
0/200
255/255
0
2
1
10
255
1
MATCHING CIRCUIT
VPI/VCI
COMMUNICATION MANAGEMENT UNIT
NOTIFY VC TO BE DELETED
+1
27
30
ATM CELL
VPI/VCI EXTRACTING UNIT

FIG.24


MESSAGE HEADER
INFORMATION ELEMENT
INFORMATION ELEMENT
INFORMATION ELEMENT
INFORMATION ELEMENT
SIGNALLING MESSAGE
TRAILER
SSCOP
TRAILER
AAL5 FRAME
ATM CELL
PTI=000 PTI=000 PTI=000 PTI=000 PTI=000 PTI=001

# FIG.25

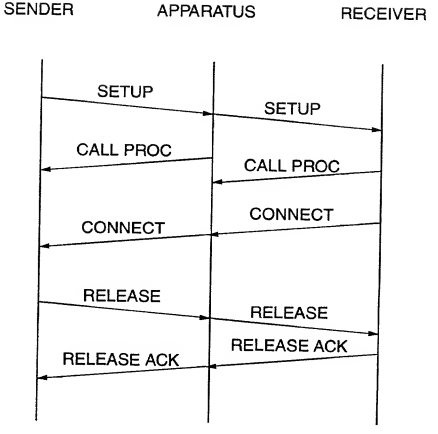

SENDER
APPARATUS
RECEIVER
SETUP
SETUP
CALL PROC
CALL PROC
CONNECT
CONNECT
RELEASE
RELEASE
RELEASE ACK
RELEASE ACK

FIG.26

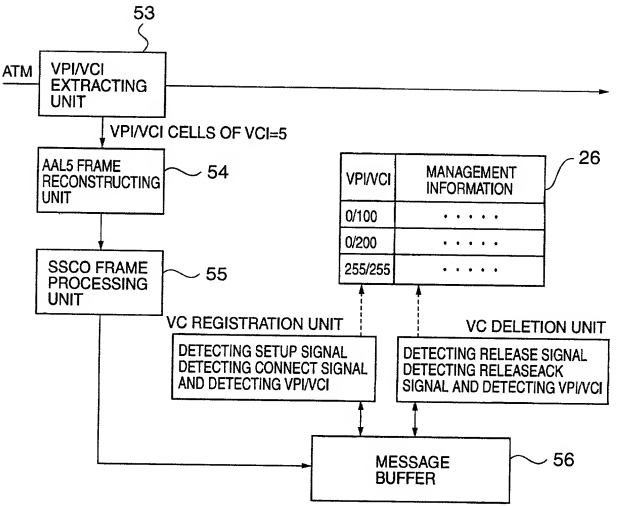

53
ATM
VPI/VCI EXTRACTING UNIT
VPI/VCI CELLS OF VCI=5
AAL5 FRAME RECONSTRUCTING UNIT
54
SSCO FRAME PROCESSING UNIT
55
VPI/VCI
MANAGEMENT INFORMATION
26
0/100
0/200
255/255
VC REGISTRATION UNIT
DETECTING SETUP SIGNAL DETECTING CONNECT SIGNAL AND DETECTING VPI/VCI
VC DELETION UNIT
DETECTING RELEASE SIGNAL DETECTING RELEASEACK SIGNAL AND DETECTING VPI/VCI
MESSAGE BUFFER
56

FIG.27

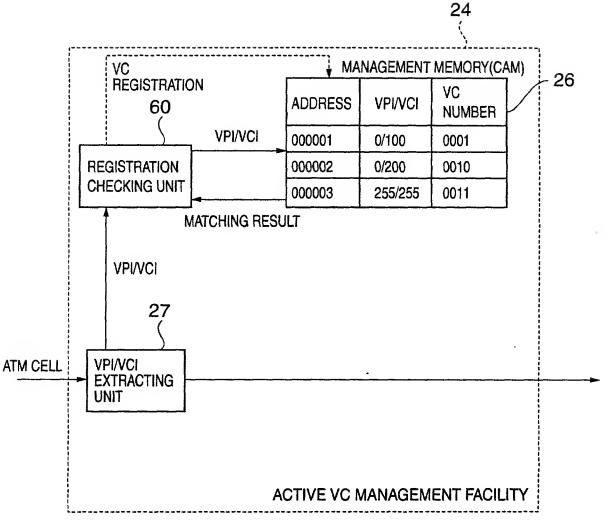

24
VC
REGISTRATION
60
MANAGEMENT MEMORY(CAM)
26
ADDRESS
VPI/VCI
VC
NUMBER
000001
0/100
0001
000002
0/200
0010
000003
255/255
0011
VPI/VCI
REGISTRATION
CHECKING UNIT
MATCHING RESULT
VPI/VCI
27
ATM CELL
VPI/VCI
EXTRACTING
UNIT
ACTIVE VC MANAGEMENT FACILITY

FIG.28

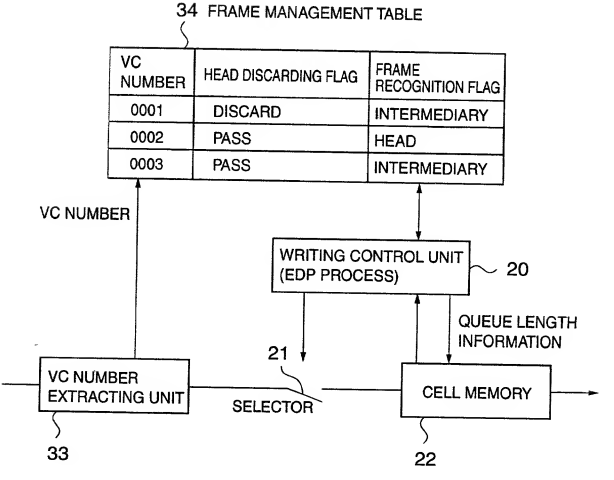

34 FRAME MANAGEMENT TABLE
VC NUMBER
HEAD DISCARDING FLAG
FRAME RECOGNITION FLAG
0001
DISCARD
INTERMEDIARY
0002
PASS
HEAD
0003
PASS
INTERMEDIARY
VC NUMBER
WRITING CONTROL UNIT (EDP PROCESS)
20
QUEUE LENGTH INFORMATION
21
VC NUMBER EXTRACTING UNIT
SELECTOR
CELL MEMORY
33
22

FIG.29

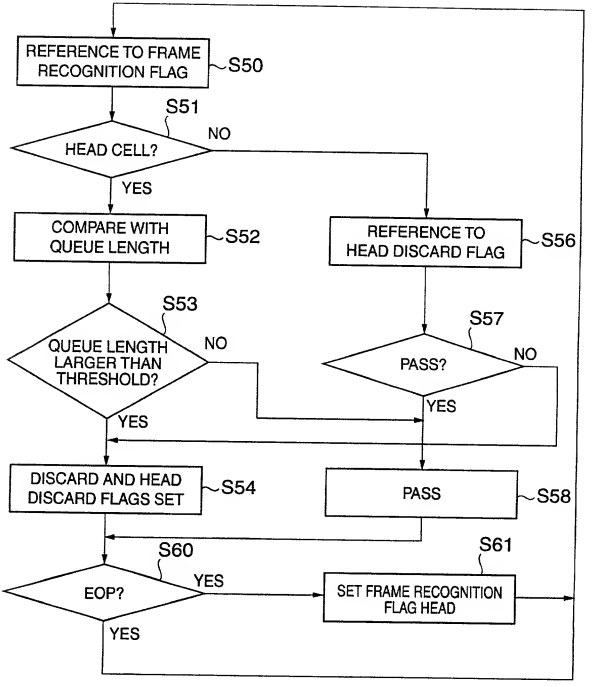

REFERENCE TO FRAME RECOGNITION FLAG
S50
S51
HEAD CELL?
NO
YES
COMPARE WITH QUEUE LENGTH
S52
REFERENCE TO HEAD DISCARD FLAG
S56
S53
QUEUE LENGTH LARGER THAN THRESHOLD?
NO
S57
PASS?
NO
YES
YES
DISCARD AND HEAD DISCARD FLAGS SET
S54
PASS
S58
S60
S61
EOP?
YES
SET FRAME RECOGNITION FLAG HEAD
YES

FIG.30

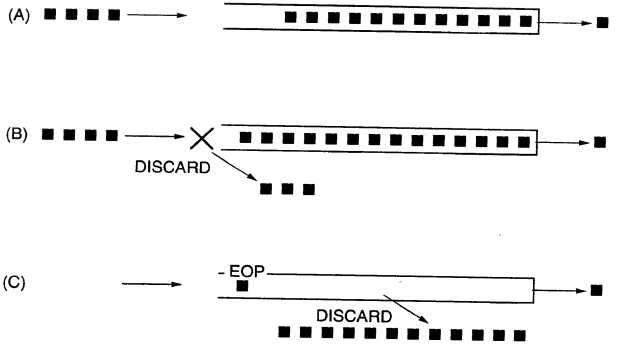


FIG.31

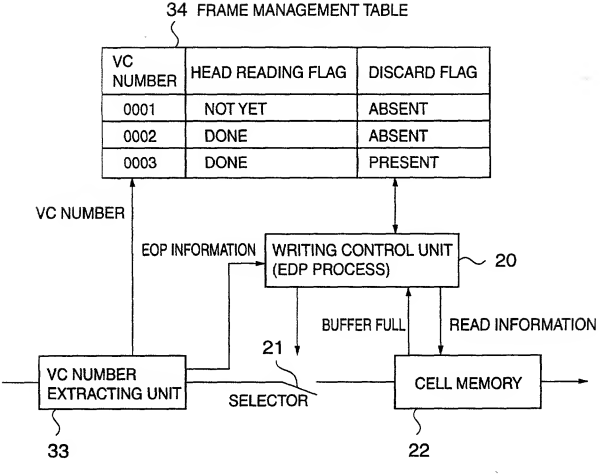

34 FRAME MANAGEMENT TABLE
VC NUMBER
HEAD READING FLAG
DISCARD FLAG
0001
NOT YET
ABSENT
0002
DONE
ABSENT
0003
DONE
PRESENT
VC NUMBER
EOP INFORMATION
WRITING CONTROL UNIT (EDP PROCESS)
20
BUFFER FULL
READ INFORMATION
21
VC NUMBER EXTRACTING UNIT
SELECTOR
CELL MEMORY
33
22

FIG.32

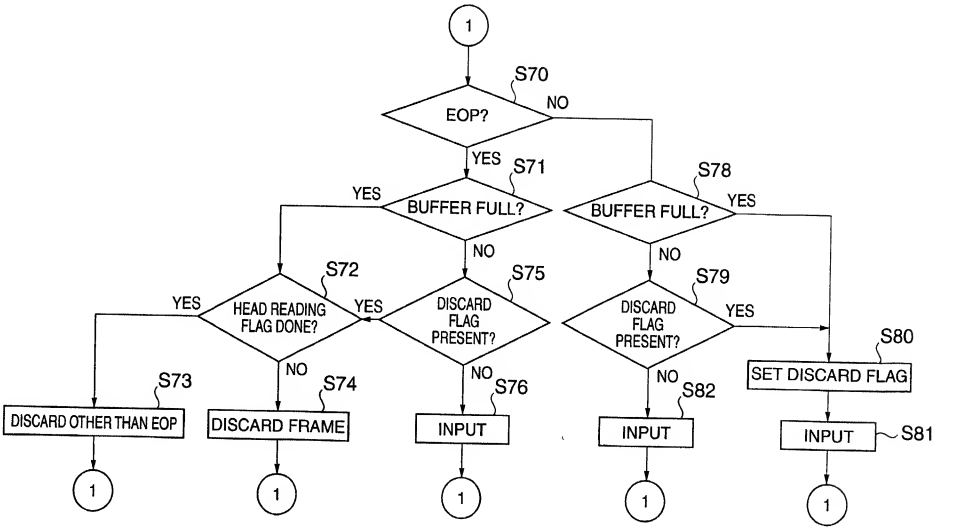

1
S70
EOP?
NO
YES
S71
BUFFER FULL?
YES
NO
S72
HEAD READING FLAG DONE?
YES
NO
S73
DISCARD OTHER THAN EOP
S74
DISCARD FRAME
S75
DISCARD FLAG PRESENT?
YES
NO
S76
INPUT
S78
BUFFER FULL?
YES
NO
S79
DISCARD FLAG PRESENT?
YES
NO
S82
INPUT
S80
SET DISCARD FLAG
INPUT
S81
1
1
1
1
1

FIG.33

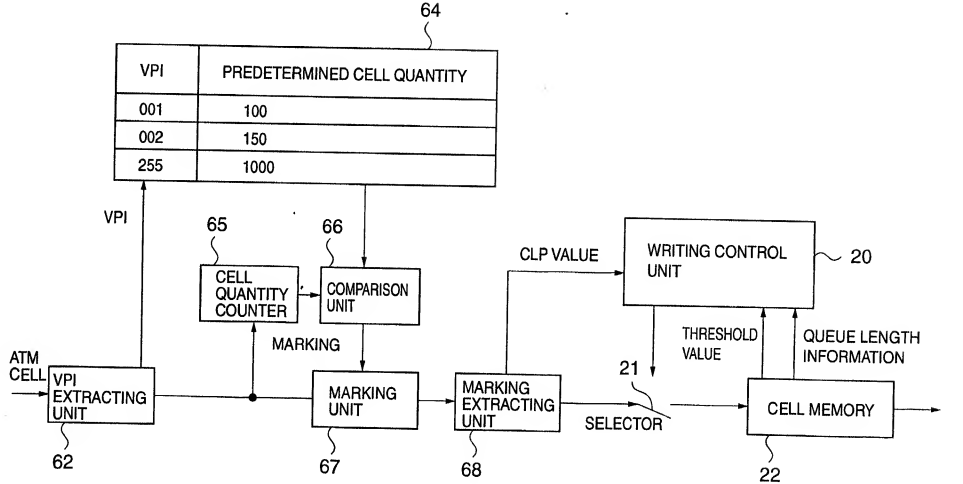
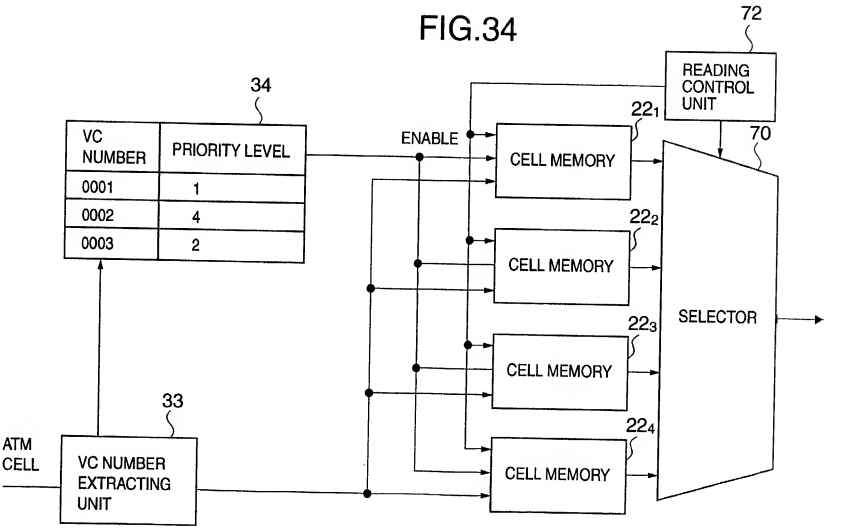

64
VPI
PREDETERMINED CELL QUANTITY
001
100
002
150
255
1000
VPI
65
66
CELL QUANTITY COUNTER
COMPARISON UNIT
MARKING
ATM CELL
VPI EXTRACTING UNIT
62
MARKING UNIT
67
CLP VALUE
WRITING CONTROL UNIT
20
THRESHOLD VALUE
QUEUE LENGTH INFORMATION
21
MARKING EXTRACTING UNIT
68
SELECTOR
CELL MEMORY
22

FIG.34


72
READING CONTROL UNIT
34
VC NUMBER
PRIORITY LEVEL
0001
1
0002
4
0003
2
ENABLE
$22_1$
CELL MEMORY
70
$22_2$
CELL MEMORY
SELECTOR
$22_3$
CELL MEMORY
33
ATM CELL
VC NUMBER EXTRACTING UNIT
$22_4$
CELL MEMORY

# FIG.35

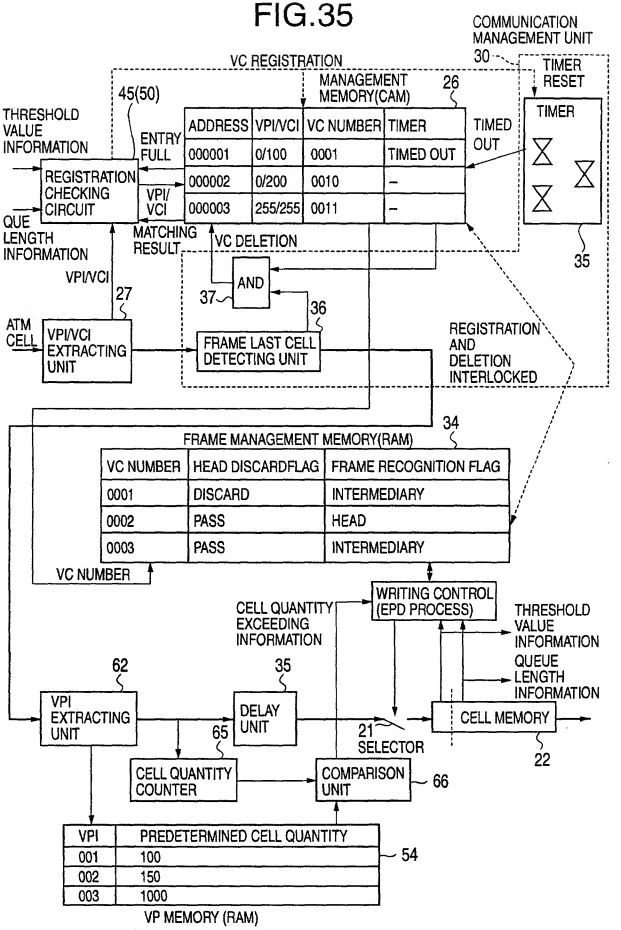
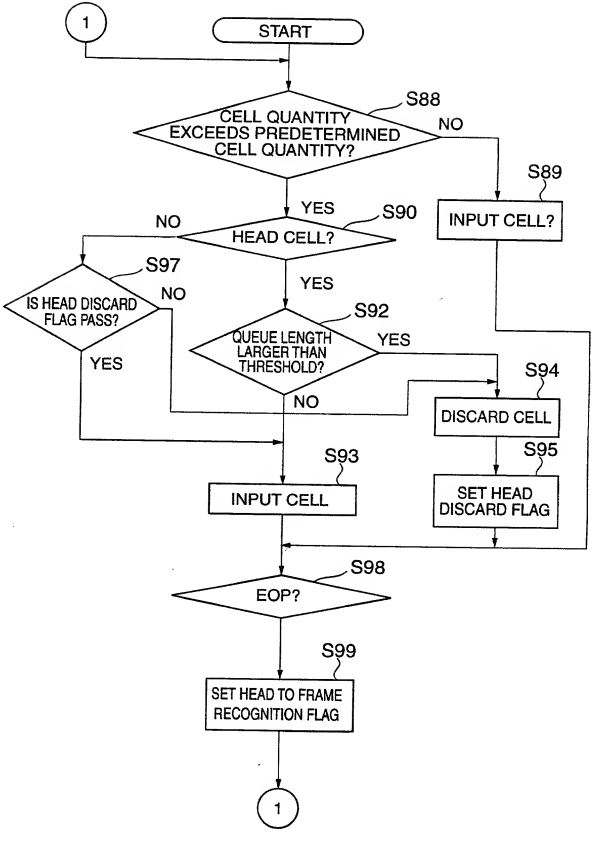
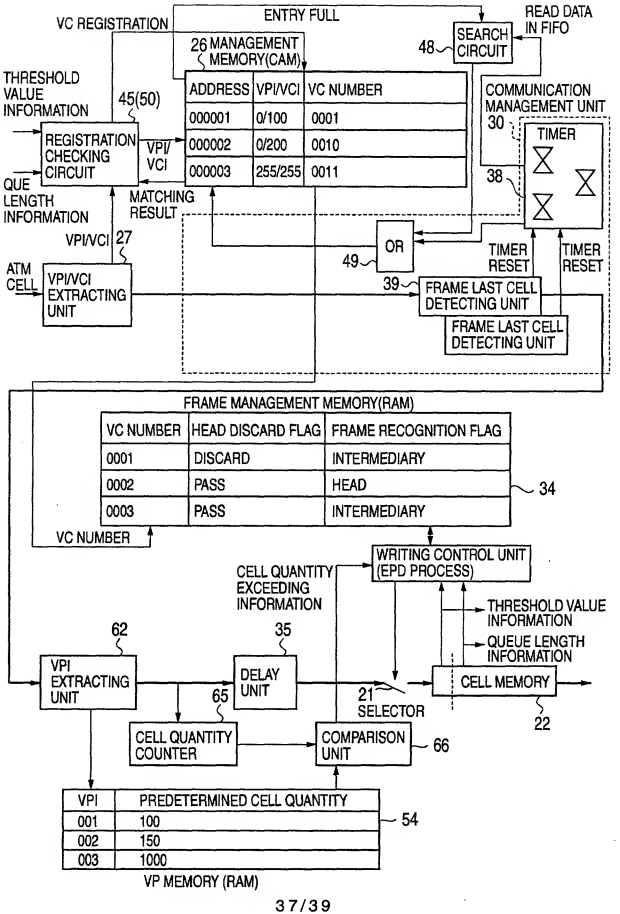

COMMUNICATION MANAGEMENT UNIT
30
VC REGISTRATION
MANAGEMENT MEMORY(CAM)
26
TIMER RESET
TIMER
45(50)
THRESHOLD VALUE INFORMATION
ENTRY FULL
ADDRESS
VPI/VCI
VC NUMBER
TIMER
TIMED OUT
000001
0/100
0001
TIMED OUT
000002
0/200
0010
–
000003
255/255
0011
–
REGISTRATION CHECKING CIRCUIT
VPI/VCI
QUE LENGTH INFORMATION
MATCHING RESULT
VC DELETION
35
VPI/VCI
27
AND
37
36
ATM CELL
VPI/VCI EXTRACTING UNIT
FRAME LAST CELL DETECTING UNIT
REGISTRATION AND DELETION INTERLOCKED
34
FRAME MANAGEMENT MEMORY(RAM)
VC NUMBER
HEAD DISCARDFLAG
FRAME RECOGNITION FLAG
0001
DISCARD
INTERMEDIARY
0002
PASS
HEAD
0003
PASS
INTERMEDIARY
VC NUMBER
WRITING CONTROL (EPD PROCESS)
CELL QUANTITY EXCEEDING INFORMATION
THRESHOLD VALUE INFORMATION
QUEUE LENGTH INFORMATION
62
35
VPI EXTRACTING UNIT
DELAY UNIT
CELL MEMORY
21
SELECTOR
22
65
CELL QUANTITY COUNTER
COMPARISON UNIT
66
VPI
PREDETERMINED CELL QUANTITY
001
100
002
150
003
1000
54
VP MEMORY (RAM)

FIG.36

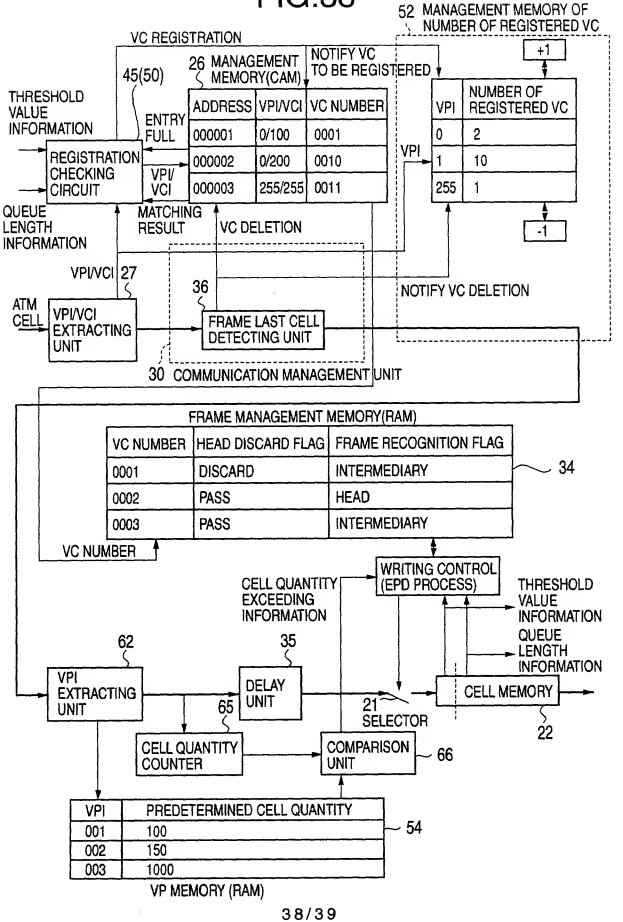



NOT ENCRYPT

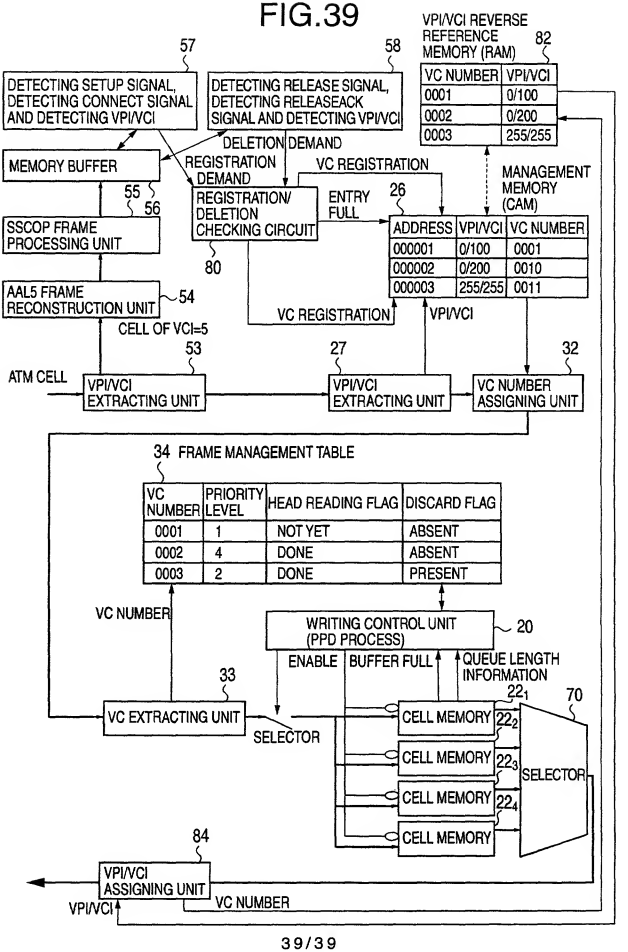
# FIG.37


VC REGISTRATION
ENTRY FULL
READ DATA IN FIFO
26 MANAGEMENT MEMORY(CAM)
48 SEARCH CIRCUIT
THRESHOLD VALUE INFORMATION
45(50)
ADDRESS | VPI/VCI | VC NUMBER
000001 | 0/100 | 0001
000002 | 0/200 | 0010
000003 | 255/255 | 0011
COMMUNICATION MANAGEMENT UNIT
30
TIMER
38
REGISTRATION CHECKING CIRCUIT
VPI/VCI
QUE LENGTH INFORMATION
MATCHING RESULT
VPI/VCI 27
OR
49
TIMER RESET
TIMER RESET
ATM CELL
VPI/VCI EXTRACTING UNIT
39
FRAME LAST CELL DETECTING UNIT
FRAME LAST CELL DETECTING UNIT
FRAME MANAGEMENT MEMORY(RAM)
VC NUMBER | HEAD DISCARD FLAG | FRAME RECOGNITION FLAG
0001 | DISCARD | INTERMEDIARY
0002 | PASS | HEAD
0003 | PASS | INTERMEDIARY
34
VC NUMBER
WRITING CONTROL UNIT (EPD PROCESS)
CELL QUANTITY EXCEEDING INFORMATION
THRESHOLD VALUE INFORMATION
QUEUE LENGTH INFORMATION
62
35
VPI EXTRACTING UNIT
DELAY UNIT
65
21 SELECTOR
CELL MEMORY
22
CELL QUANTITY COUNTER
COMPARISON UNIT
66
VPI | PREDETERMINED CELL QUANTITY
001 | 100
002 | 150
003 | 1000
54
VP MEMORY (RAM)

# FIG.38


52 MANAGEMENT MEMORY OF NUMBER OF REGISTERED VC
VC REGISTRATION
45(50)
26 MANAGEMENT MEMORY(CAM)
NOTIFY VC TO BE REGISTERED
+1
THRESHOLD VALUE INFORMATION
ENTRY FULL
ADDRESS
VPI/VCI
VC NUMBER
000001
0/100
0001
000002
0/200
0010
000003
255/255
0011
VPI
NUMBER OF REGISTERED VC
0
2
1
10
255
1
-1
REGISTRATION CHECKING CIRCUIT
VPI/VCI
QUEUE LENGTH INFORMATION
MATCHING RESULT
VC DELETION
VPI/VCI 27
36
NOTIFY VC DELETION
ATM CELL
VPI/VCI EXTRACTING UNIT
FRAME LAST CELL DETECTING UNIT
30 COMMUNICATION MANAGEMENT UNIT
FRAME MANAGEMENT MEMORY(RAM)
VC NUMBER
HEAD DISCARD FLAG
FRAME RECOGNITION FLAG
0001
DISCARD
INTERMEDIARY
34
0002
PASS
HEAD
0003
PASS
INTERMEDIARY
VC NUMBER
WRITING CONTROL (EPD PROCESS)
CELL QUANTITY EXCEEDING INFORMATION
THRESHOLD VALUE INFORMATION
QUEUE LENGTH INFORMATION
62
35
VPI EXTRACTING UNIT
DELAY UNIT
CELL MEMORY
65
21
SELECTOR
22
CELL QUANTITY COUNTER
COMPARISON UNIT
66
VPI
PREDETERMINED CELL QUANTITY
001
100
54
002
150
003
1000
VP MEMORY (RAM)

# FIG.39


VPI/VCI REVERSE REFERENCE MEMORY (RAM)
82
VC NUMBER
VPI/VCI
0001
0/100
0002
0/200
0003
255/255
57
DETECTING SETUP SIGNAL, DETECTING CONNECT SIGNAL AND DETECTING VPI/VCI
58
DETECTING RELEASE SIGNAL, DETECTING RELEASEACK SIGNAL AND DETECTING VPI/VCI
DELETION DEMAND
MEMORY BUFFER
REGISTRATION DEMAND
VC REGISTRATION
MANAGEMENT MEMORY (CAM)
55
56
REGISTRATION/ DELETION CHECKING CIRCUIT
ENTRY FULL
26
SSCOP FRAME PROCESSING UNIT
80
ADDRESS
VPI/VCI
VC NUMBER
000001
0/100
0001
000002
0/200
0010
000003
255/255
0011
AAL5 FRAME RECONSTRUCTION UNIT
54
VC REGISTRATION
VPI/VCI
CELL OF VCI=5
ATM CELL
53
27
32
VPI/VCI EXTRACTING UNIT
VPI/VCI EXTRACTING UNIT
VC NUMBER ASSIGNING UNIT
34 FRAME MANAGEMENT TABLE
VC NUMBER
PRIORITY LEVEL
HEAD READING FLAG
DISCARD FLAG
0001
1
NOT YET
ABSENT
0002
4
DONE
ABSENT
0003
2
DONE
PRESENT
VC NUMBER
WRITING CONTROL UNIT (PPD PROCESS)
20
ENABLE
BUFFER FULL
QUEUE LENGTH INFORMATION
33
22 1
70
VC EXTRACTING UNIT
SELECTOR
CELL MEMORY
22 2
CELL MEMORY
22 3
SELECTOR
CELL MEMORY
22 4
CELL MEMORY
84
VPI/VCI ASSIGNING UNIT
VPI/VCI
VC NUMBER